

Very low computational complexity (VLCC) architecture for optical interconnect in Data Center Networks

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Summary

Real time cloud computing applications require a low latency network. The latency of optical interconnect in Data Center Networks (DCNs) is dependent on the complexity of routing algorithm. The routing algorithm makes decisions about the forwarding of a packet on each successive node. If a routing algorithm is more complex, it requires more hardware resources to implement; which incurs extra cost and latency to the optical interconnect. This paper analyzes the complexity of existing architectures for the first time by showing Big O notation of complexity for each architecture. Different factors affecting the computational complexity of any routing algorithm are identified.

This paper proposes a new architecture named VLCC. It has very low fixed routing complexity irrespective of network size. It has no packet loss at network layer under many to many and all to one communication pattern. The only packet loss is at physical layer due to signal degradation caused by optical components. The level of signal degradation is analyzed in terms of received signal power, bit error rate (BER), receiver sensitivity, path loss, and blocking probability. VLCC architecture is highly suitable for real time applications that require deterministic quality of service (QoS), where network performance is not affected by the traffic pattern.

Keywords: Optical Interconnects, Data Center Networks, Computational Complexity

1 Introduction

Cloud and the web-based services need a high network performance. Ensuring certain QoS requires extra routing control in the network and careful utilization of network resources. To utilize the network resources efficiently, an intelligent routing algorithm is needed, which adds the complexity. The factors which influence the computational complexity of optical DCNs include reconfigurability, number of active optical components that need to be controlled, and the number of nodes in the network. The amount of data being used by data centers is continuously increasing. The data center must efficiently process a huge amount of data efficiently. A large amount of data is transferred for

migration, data sharing, and communication. To improve the performance, the network latency must be kept to the minimum, which requires efficient routing and reduction in the complexity of routing algorithm (1).

The VLCC architecture is proposed which has very low routing complexity and non-blocking capability is proposed. Due to non-blocking nature of the optical interconnect, it ensures very low latency. Packet loss increases the latency because each lost packet needs to be retransmitted. Retransmission of packets may involve store and forward mechanism.

The contribution of the paper includes the analysis of the routing algorithm complexity of existing architectures, identification of factors affecting the routing complexity and the proposal of a new architecture.

Section II discusses the architectures in the literature that have centralized control and their computational complexity, section III discusses VLCC architecture, section IV discusses simulation setup, Section V discusses performance in terms of complexity of routing algorithms, capacity of the CDMA, scalability, cost, packet loss, and signal degradation.

Section VI ends up with conclusions.

2 Complexity of existing centralized control architectures

Optical interconnects can be categorized into two broad categories with respect to control, optical interconnects with centralized and distributed control. The control algorithm of optical interconnects having centralized control is implemented in electronics. The analysis of the complexity of control algorithms of architectures having centralized architectures is the focus of this paper. The control algorithm of architectures having distributed control is very simple and has very limited affect on the latency, scalability, and implementation. The architectures in the literature that have centralized control include Proteus, DOS, OSMOSIS, and OFDM.

2.1 Proteus

In Proteus (3), a topology malleable architecture is proposed. This is shown in Figure 1. Major optical components used in Proteus include wavelength selective switch(WSS), optical circulator, optical crossbar, and optical transceivers. The optical components that need to be controlled by the routing algorithm include WSS and optical crossbar. Top of Rack (ToR) switch is used to connect nodes and every node has a unique wavelength. These wavelengths are combined using the multiplexer and sent to WSS. WSS gets instructions from the topology manager(TM) to group the wavelengths that have the packets for same destination ToR switch. Groups of wavelengths are sent to optical crossbar, which directs the to respective destination ToRs. TM informs optical crossbar to send the wavelength groups to a particular destination ToR. If K is the number of ToRs and N is the total number of nodes in the network then each ToR has $\frac{N}{K}$ nodes. The number of WSS is equal to the number of ToRs. If each WSS has W ports then MEMS should have KW ports. W ToRs can be reached by each sending ToR simultaneously (6).

The algorithm in Proteus is given below

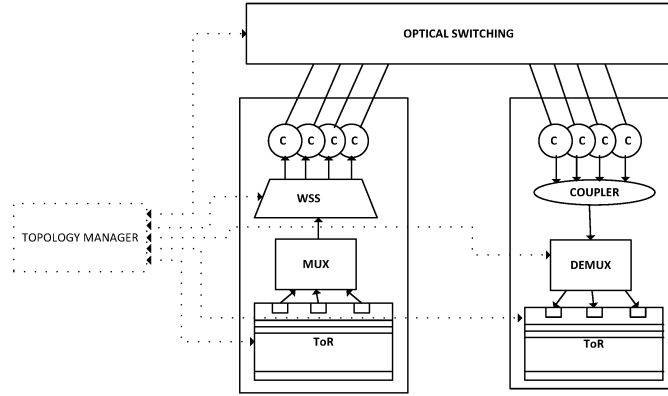


Figure 1: Proteus architecture

- 1. Assignment of elephant flows:** High volume flows are elephant flows. High volume flows are identified. If the data volume exceeds the capacity of a single wavelength then multiple wavelengths are assigned to this flow and directed to MEMS circuit links via WSS. Each ToR has N/K nodes. It needs to sort the traffic of N/K nodes with respect to the volume of traffic. The asymptotic complexity is $O(\frac{N}{K})^2$.
- 2. Achieve connectivity:** Next step is to achieve connectivity between the ports of the optical crossbar. Edge exchange operation is needed to change the previous configuration. If optical crossbar has $K \times W$ ports, then $K \times W$ instructions would be needed to set the edges of each port. The asymptotic complexity of this operation would be $O(K \times W)$.
- 3. Identification of paths:** When the optical crossbar configuration and connectivity is known, routes need to be found by routing scheme using shortest path. If Dijkstra's algorithm is used, it requires $E + v \log(v)$ instructions. The number of edges in Proteus is $2 \times (K + K \times W)$ and the number of vertices is $2 \times (K + W + 1)$. The asymptotic complexity for this step according to Dijkstra's algorithm would be $O(K \times W)$.
- 4. Compute capacity demands:** This architecture can produce N flows. All these flows need to be examined to compute the capacity demands of internal links of MEMS switch. The complexity of this step is $O(N)$.
- 5. Assign wavelengths λ s:** Each ToR has λ wavelengths, that would be ideally assigned to $\frac{N}{K}$ flows on that ToR. In case some flows exceed the capacity of a single wavelength, then multiple wavelengths will be assigned. $\frac{N}{K}$ flows will be scanned and assigned wavelengths for each rack. When assigned wavelength counter exceeds λ , the process will be stopped. The complexity of this step would be $O(\frac{N}{K})$.

Over all complexity = $O(\frac{N \times W}{K})$

2.2 DOS

In DOS (9), two main optical components are used; tunable wavelength converter (TWC) and Arrayed Waveguide Grating Router (AWGR). This is shown in Figure 2. The input signal goes through the label extractor (LE), which extracts the header from the packet and sends it to the control plane. The payload waits in fiber delay line (FDL) until the routing decision of control plane reaches the TWC. To route a particular input to some output port, the wavelength of the signal is changed through TWC. The wavelength conversion at TWC is based on the destination address. The routing path inside AWG is based on the wavelength of the signal. To receiver multiple flows a demultiplexer is used at the output port (6).

DOS uses a 1:D optical demultiplexer and $N \times N$ AWGR for N I/O ports. If $D=N$, there is no contention at the

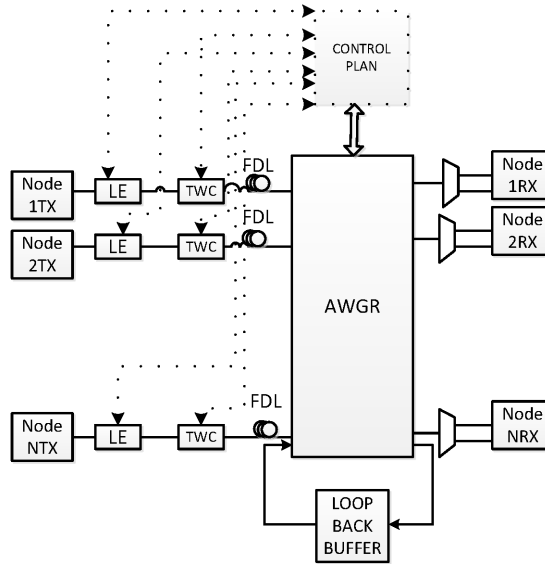


Figure 2: DOS architecture

output port. However if $D < N$ then more than two packets will reach the same demultiplexer output port and none of them is received correctly. Wave group manager in the control plane is responsible for deciding when a grant will be made based on packet length and last distribution of grants. To resolve the contention for $D < N$ case, arbitration is needed, such that at most D packets with D different wavelengths arrive at a particular AWGR port. Arbitration is done by dividing the entire set of wavelengths into wave groups. The number of wavelengths in one group is $M=N/D$. Input ports using the wavelengths from a single group form a contention group. The wavelengths from different wave groups do not contend as the wavelengths of different wave groups come out from different outputs of optical demultiplexer. The arbitration in DOS is dependent upon the size of wave group. There are two types of connection requests, one being serviced from the previous iteration known as active requests and the new arrivals known as

current requests. Current requests are compared using the wavelength routing table with previous active requests for contention. If there is no contention grant is allocated. In worst case, there will be N current requests and N active requests. Each request will be checked for contention within the same wave group with active requests and current requests. Active requests have high priority, if any of current request has conflict with active requests then current request is blocked. If two current requests have contention then the request with lower priority is blocked. There will be D comparisons for each of N current requests and N active requests. The asymptotic complexity of control algorithm in DOS will be $O(DN)$. The computational complexity of DOS is dependent on two factors; ports of receiver demultiplexer and number of nodes.

2.3 OSMOSIS

In OSMOSIS (8), a broadcast and select architecture is used that employs a combination of wavelength and space division multiplexing. In order to avoid a collision, packets are stored temporarily in the ingress adapter VOQs. All the packets that have reached the head of VOQ across all ingress adapters are the candidates for transmission across the switch. The scheduler must determine the best combination of requests in such a way that no more than one packet is scheduled to the same output at any given time. Figure 3 shows that input data streams are combined using wavelength and space multiplexing by combining their data on different of wavelengths and groups of fiber. The contents of groups are broadcast to all output ports through star couplers. The select units on the output side feed the egress adapters in a pairwise manner. The select unit uses first stage of SOA gates to select correct fiber and the second stage of SOA gates selects correct wavelength within that fiber. (6).

In OSMOSIS Fast Low Latency Parallel Pipelined Arbitration (FLPPR) algorithm (2) is used. There are N pipeline

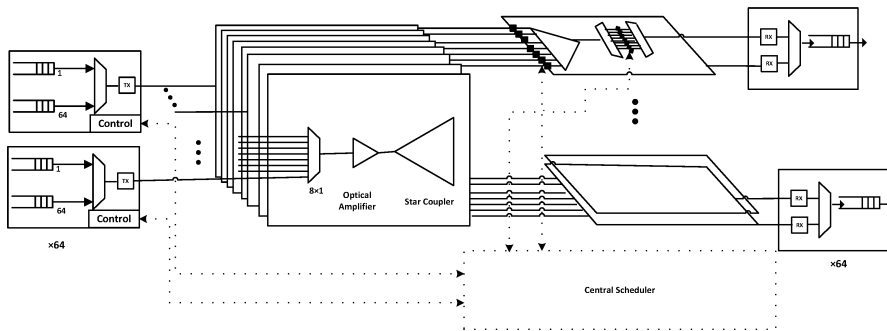


Figure 3: OSMOSIS architecture

stages with one allocator per stage. In FLPPR, the arbiter computes matching between inputs and outputs every time slot. This scheme employs N allocators, each of which corresponds to an input port. Every stage maintains

a match matrix which indicates which input and outputs have been matched. Every input port has VOQs. Every allocator checks the previous allocator for the occupied ports. If a port is already occupied by the previous allocator, the match is not found. The probability of match decreases as we go to higher stages. Every stage updates the match matrix. If the VOQ of a port is already serviced then it's round robin counter is incremented. Every allocator executes a part of it and passes the results to next allocator. To reduce latency N requests can be sent in parallel and the result is collected one by one in every cycle. If arrays are used to stores the results of matching then the complexity of this architecture becomes $O(N^2)$ (2).

2.4 OFDM

In Orthogonal Frequency Division Multiplexing (OFDM) (7), cyclic arrayed waveguide grating (CAWG) is the key component, as shown in Figure 4. Each input port can communicate with all the output ports simultaneously. Each of the CAWG port is connected to a ToR, this allows each ToR to send data to all other ToRs at the same time. The inter rack signal is aggregated and each OFDM modulator aggregates the signal into OFDM signal with the assignment of sub-carriers. The wavelength arrangement of CAWG allows the WDM channels to be routed to respective output ports. The sub-carrier assignment is performed by using a central scheduler (6). Each ToR evaluates the requested

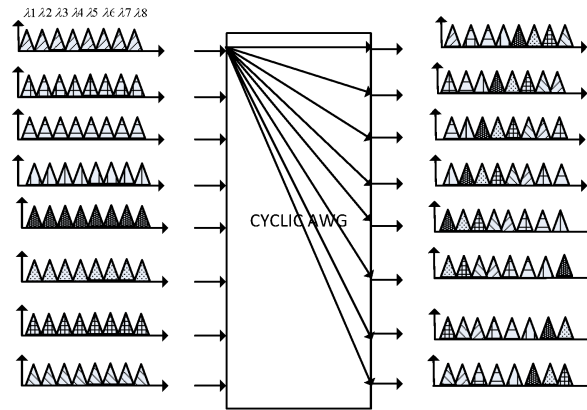


Figure 4: OFDM architecture

sub-carriers for specific ports based on traffic and sends the demand for requested sub-carriers to the central scheduler through control packet. The scheduler divides the sub-carriers requested by each input port for an output port by the total sub-carriers requested for a particular output port by all input ports. This ratio tells how much carriers need to be assigned to a particular request. The scheduler first sums up the sub-carriers requests for an output port by all the input ports. It divides the individual requests by all input ports for this output port by total requests. Sub-carriers are assigned based on this ratio. The overall complexity of this architecture will be $O(N)$.

3 VLCC architecture

The VLCC architecture has very low (constant) complexity. It exploits three dimensions of multiplexing namely; code division multiple access (CDMA), wavelength division multiplexing (WDM), and space division multiplexing(SDM). WDM allows different optical channels having different wavelengths to be sent on the same fiber. WDM advantages include cost reduction, increase in capacity of fiber, transmission of different modulation formats and channel expansion after network deployment. In WDM system the performance of WDM multiplexer/demultiplexer is a primary consideration(11). Filters are needed in WDM optical systems to select wavelength channels from WDM signal. Channels are directed on separate outputs using wavelength multiplexers and demultiplexers (10). WDM effectively provides multiple transmission lines over a single fiber. WDM systems show the better utilization of bandwidth.

CDMA is a popular method of optical access. Each user is assigned a code which can be sent on the same fiber. The advantages of CDMA are security, capacity scalability on demand, asynchronous transmission, and no existence of packet collision(12). CDMA system has lower latency than TDMA. It operates asynchronously without any central control (13). In CDMA, each bit is divided into n time periods. Each user has a unique code. 0 bit is sent using all zeros sequence and 1 bit is sent using code. This is spread spectrum technique which increases the bandwidth of data. CDMA provides a mechanism to share same bandwidth among many users. The use time spreading and codes allow to increase the number of users than available bandwidth. CMDA simplifies the network control and management. There is no need for a centralized clock to arbitrate channel contention. Users can be added by adding a new code. If extra codes are not available, then the network can add new users by the increase in the wavelength or time domain spreading (15). The interference between codes of same channel is multiple access interference (MAI). Dominant source of error in CDMA is MAI. The utilization of the number of codes in the channel is limited by MAI. Code-word sequence is important to reduce the impact of MAI. An other type of CDMA is spectral amplitude CDMA. In spectral amplitude CDMA, the spectrum is divided into N slices, which are masked by to the code of each user. Coded spectrum and the complement of it are used to send binary information(14).

SDM is used to establish spatial paths through same fiber or multiple parallel fibers. SDM networks use spatial channels or groups of wavelength to be transmitted on separate fibres or spatial modes (16). SDM is used in VLCC architecture during the broadcast stage. The data of a single rack is broadcasted to multiple racks on separate fibers using SDM.

The proposed architecture is shown in Figure 5. The workflow of VLCC architecture can be divided into various stages which include i) address assignment stage, ii) multiplexing stage, iii) broadcast stage iv) demultiplexing stage, and v) destination select stage. This is shown in Figure 6. Each stage in workflow is explained below.

Address assignment stage: Each node has a unique address which consists of wavelength, CDMA code, and its location in space. The nodes are divided into racks to allow the re-use of CDMA codes. The number of nodes in a

rack is dependent on the number CDMA codes, number of wavelengths, and size of coupler. The number of racks in the network is dependent on the size of the splitter and the total number of wavelengths.

Multiplexing stage: The nodes along wavelength dimension are multiplexed using an optical multiplexer and the node along code dimension are combined using the coupler on to a single fiber. The output of coupler contains the data of all the nodes of that rack.

Broadcast stage: Each rack has packets that need to go to different destination racks. The combined data of all nodes on a single fiber is broadcast to all racks using a splitter. Splitter creates multiple copies of the same optical signal for all destination racks.

Demultiplexing stage: When this optical signal reaches destination racks, the wavelength channels are separated using wavelength demultiplexer. Each wavelength channel has many coded CDMA streams. Same wavelengths containing different CDMA codes, which are also demultiplexed using CDMA

Destination select stage: In last stage, the packets are forwarded to the destination address through 1×64 optical switch. This is the only part of the network that involves control.

The VLCC architecture eliminates the routing algorithm by using the concept of broadcast. The data of a single transmitter rack reaches all the racks through broadcasting using splitters. The code and wavelength multiplexed data is demultiplexed at receiver rack. No routing algorithm or intelligence is needed so far. Only a single routing decision is needed at 1×64 space switch, which is constant. This makes the algorithmic complexity of this architecture to be $O(1)$.

4 Simulation Setup

Optical DCN can be simulated using OptiSystem software (18). Light path of each architecture is modeled in terms of the number and type of optical components encountered in the way of the optical signal. Each optical component is treated as the node of a complex network and optical signal communicated between the nodes represents the edges. This type of relationship is shown in Figure 7. The simulation in OptiSystem is done by passing the optical signal through the light path of optical data center architecture. The optical signal is a bit sequence using non-return-to-zero (NRZ) pulse generator. Mach Zehendr (MZ) modulator is used to generate an optical signal corresponding to bit stream. MZ modulator is used because of its small size, low power consumption, and monolithic integration capability with other laser components. It allows higher modulation speeds, large extinction ratios, and very low or controllable frequency chirp. The data rate of 10 Gbps and wavelength of 1638.21 nm is considered. 1638.21 nm frequency is used because it lies in the L band. L band is popular for very low attenuation (db/km) and high frequency. The data rate of 10 Gbps is used because it supports IEEE 802.3 Ethernet. This allows the transmission of data at 10 Gbps up to

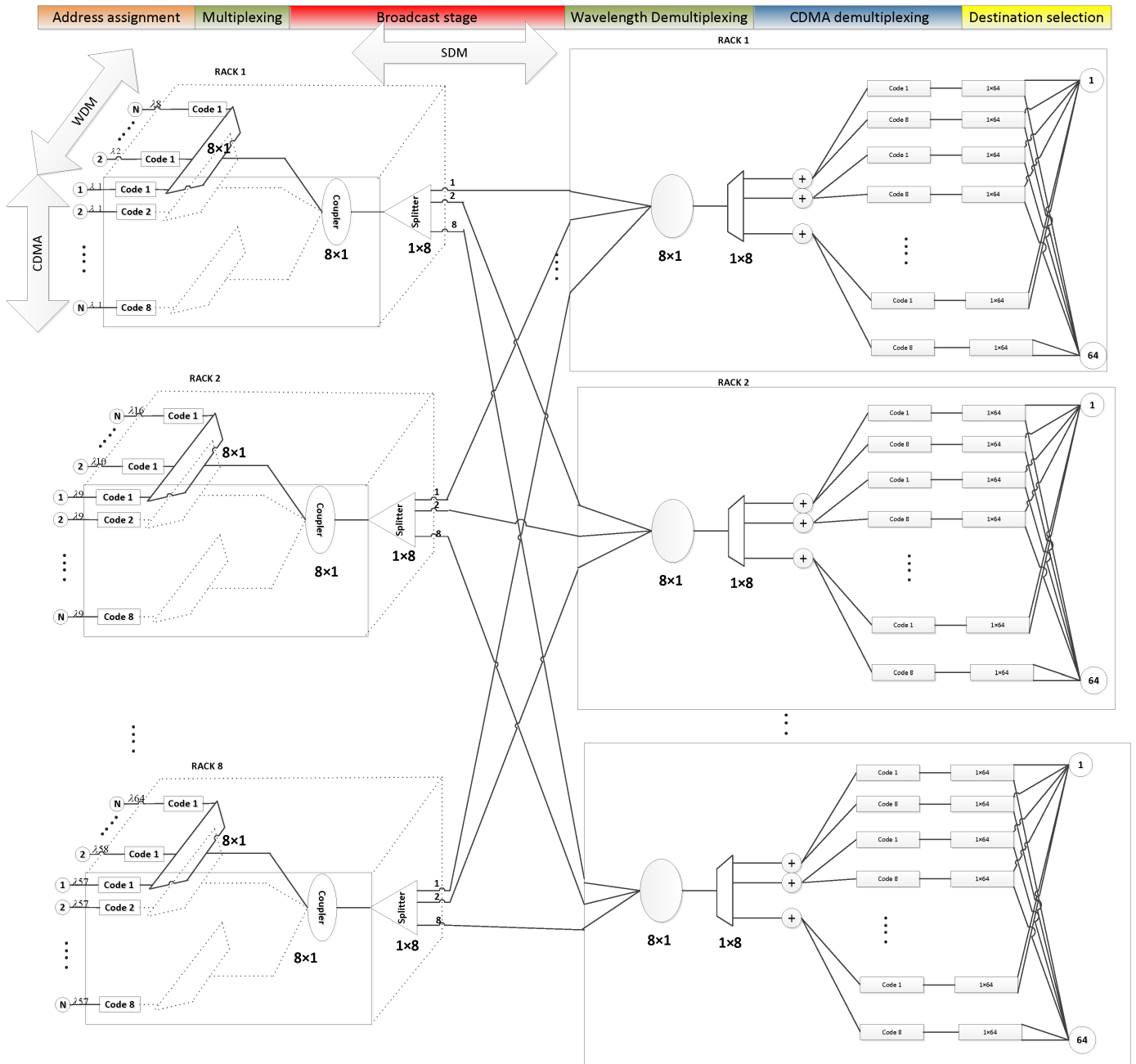


Figure 5: VLCC architecture with very low control complexity

300m. This is suitable for data center applications (5).

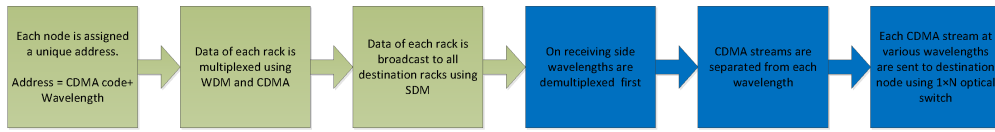


Figure 6: Work flow of VLCC architecture

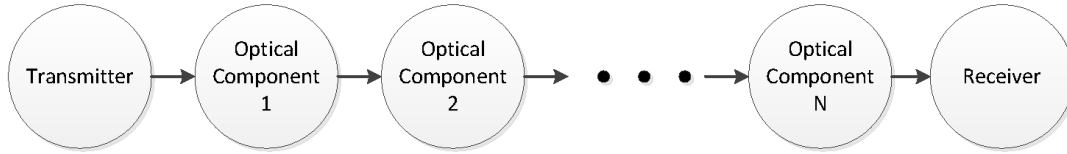


Figure 7: Light path modeled in OptiSystem to measure the signal degradation

Table 1: Parameters affecting the computational complexity

Architectures	Parameters
Proteus	Nodes , ToRs, and WSS ports.
DOS	Nodes and receiver demultiplex ports.
OSMOSIS	Nodes.
OFDM	Nodes.

5 Performance

5.1 Computational complexity

The dependence of computational complexity on different parameters for different architectures is shown in Table 1.

The computational complexity of VLCC architecture is not affected by the increase in the number of nodes. This happens because the routing of the VLCC architectures is supported by CDMA codes. The use of three multiplexing domains; frequency, space, and code simplifies the routing mechanism. On the sender side, all the information is multiplexed and no routing algorithm is needed. On the receiver, the routing is done at OCDMA demultiplexer and 1×64 switch.

The computational complexity gives an idea about the inherent nature of routing algorithm used in various architectures. This analysis is very useful for the hardware implementation of the control algorithms. The complexity of routing algorithms affects the latency of the control decision. A judgement about the latency can be made by observing the computational complexity, because if a control algorithm is more complex it requires more logic gates to be implemented in hardware which contributes towards more latency.

5.2 CDMA capacity

The bandwidth of CDMA is roughly equal to reciprocal of the chip duration (17). The proposed architecture uses 8 CDMA codes in each rack which are reused across all the racks. In order for each node to get a net bandwidth of 10 Gbps, each node should be installed with network interface cards (NIC) with a total supported bit rate of 80 Gbps. Two 40 Gbps NIC is installed on each node which is able to deliver a net 10 Gbps bandwidth under CDMA. The inter rack bandwidth of VLCC architecture is 640 Gbps.

5.3 Scalability analysis

Scalability of optical components is looked from two perspectives. One is the optical components available in the the market, that can be purchased by anyone. Other is the optical components produced by researchers, which are mentioned in the literature but not available in the market. These components are tested in research laboratories and are not available in the market. The scalability analysis here is with respect to optical components available in the market. This is shown in Figure 8.

Scalability of Proteus: On each rack, Proteus uses 32×1 multiplexer and 1×32 WSS. The 32 ports of each WSS are connected to 384×384 switching matrix. This implies that

Total number of nodes per rack = 32

Total number of racks = 12

Total number of nodes in the network = 382

Scalability of DOS: DOS is CAWG based architecture. The scalability of DOS is dependent upon the scalability of CAWG. It is limited to 40 ports.

Scalability of OSMOSIS: OSMOSIS can have 16 groups of nodes each having 32 nodes because multiplexer has a capacity of 32 nodes and coupler has 16 ports. This makes it possible to have 512 nodes.

OFDM scalability: OFDM is based on CAWG and each port of CAWG has subcarriers. CAWG has 40 ports and if each port can accommodate 2 servers. This architecture can support 80 ports.

Scalability of VLCC: In each rack, VLCC architecture has 8 codes and 8 multiplexer ports making it possible to achieve 64 nodes. The total number of racks are 8. This makes this architecture to achieve 512 ports.

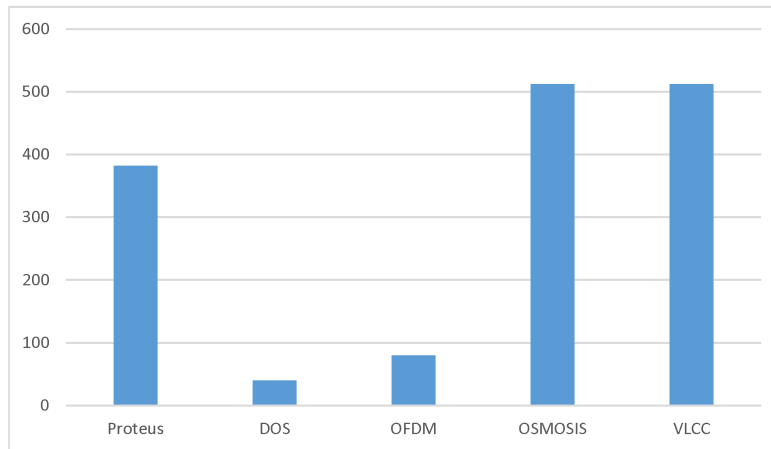


Figure 8: Scalability comparison

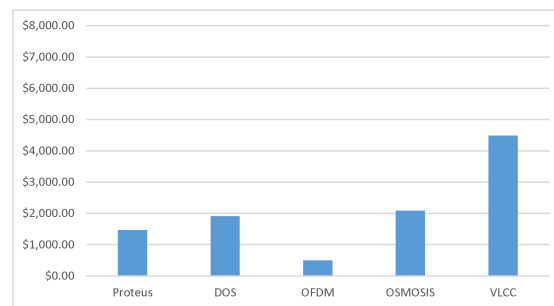


Figure 9: Cost of single port in each architecture

5.4 Cost comparison

Various optical components are used to make optical interconnects for data center networks. Each optical component has its own cost at which it can be purchased from the market. The cost of various optical components is shown in Table 2. The cost comparison of all the architectures is shown in Figure 9. This comparison is for per port cost. This Figure shows that cost of the proposed architecture is comparable to other architectures with respect to performance. The VLCC architecture has a higher cost than other counterparts because it gives several advantages over other architecture which covers the cost benefit of this architecture. The first benefit is it has a very low computational complexity of routing algorithm which makes it suitable for real time applications, the second benefit is that it shows no loss under many to many and all to one communication pattern, and third it has a low receiver sensitivity due to small signal degradation. Small signal degradation makes it possible to receive the information at low received power.

Table 2: Cost of various optical components

Optical component	Size	Cost \$
Multiplexer	32×1	890
Circulator	3 Port	130
Wavelength selective switch	1×32	7995
Switch	1×16	1590
Demultiplexer	1×32	1300
Cyclic AWG	40 Channel	2490
SOA	1 Port	630
Optical crossbar	383×383	278850
Fiber delay line	1 Port	320
FPGA	1 kit	417
TWC	1 port	700
NIC 10Gbps	1	245
NIC 40Gbps	1	360
Multiplexer	8×1	400
Splitter	1×8	30
OCDMA decoder	1×8	160

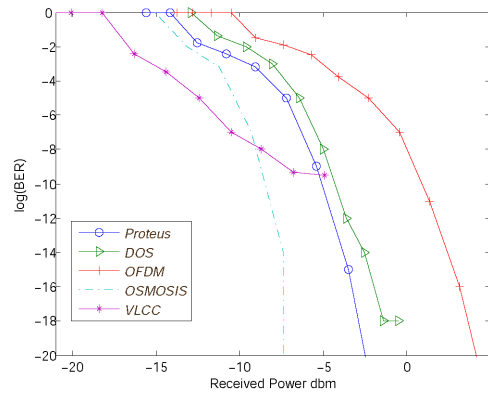


Figure 10: Received power vs BER

5.5 Signal degradation

The input power of the signal can be changed by changing the laser power of MZ modulator. BER is calculated for different received powers. Based on the signal degradation of different optical components and path loss, the received power vs BER is plotted in Figure 10. The architectures towards left-hand side of the graph show lowest signal degradation. The signal degradation in VLCC is lowest because it uses passive optical components like multiplexer, demultiplexer, splitter, and coupler etc. Passive components only affect the magnitude of the optical signal. They do not change the shape of the signal.

Path loss is the difference in transmit and received power. This is shown in Figure 11. Path loss is caused by optical components in the light path. Different optical components cause different loss to the signal. The VLCC

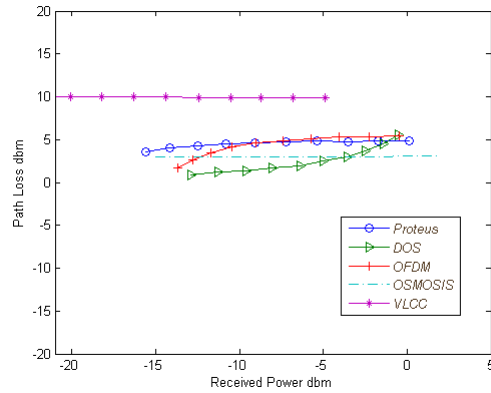


Figure 11: Path loss comparison

architecture has highest path loss due to use of couplers and splitters, but this does not affect the performance of VLCC architecture because optical components in its light path do not change the shape of the signal, which makes the signal to receivable even at lower received power.

5.6 Throughput analysis

The throughput of architectures has been compared by using 512 network for each architecture, 512 sender nodes and 512 destination nodes using NS2 network simulator(19). The example configuration of nodes and TCP flows is shown in figure 12. 300 TCP flows have been created for two communication patterns, the All to One and Many to Many communication pattern. The Many to Many communication pattern consists of 300 randomly chosen sender nodes, which send 300 TCP flows to randomly chosen destination nodes. The randomly chosen sender and destination nodes are created using Uniform random variable The throughput results for Many to Many communication pattern are shown in Figure 13. The All to One communication pattern consists of 300 sender nodes, which communicate with single destination node. The throughput performance of architectures for All to One communication pattern is shown in Figure 14. The VLCC architecture outperforms all architectures in All to One communication pattern. All to One communication pattern is the worst communication pattern that can arise in any communication network.

6 Conclusions

It is concluded from the analysis of existing architectures that the computational complexity of the control algorithms in optical interconnects for DCNs is dependent upon i) reconfigurability ii) number of active components iii) high radix requirement. This is shown in Figure 15.

i) Reconfigurability Traffic of a DCN is highly malleable in nature (3). Due to highly changing traffic patterns between long and short flows, the architectures should utilize circuit switching for long flows and packet switching

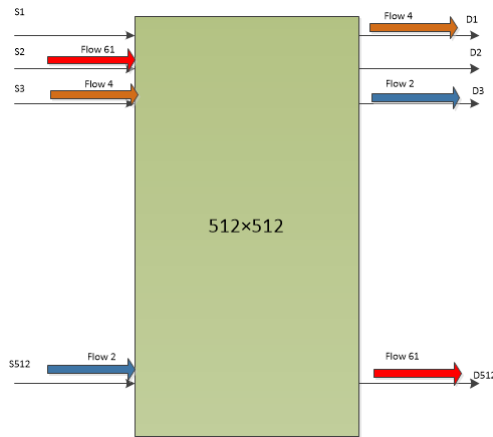


Figure 12: Simulation setup in NS2

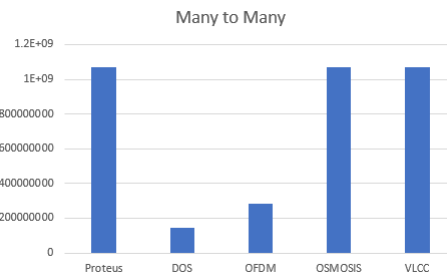


Figure 13: Throughput comparison for Many to Many Communication pattern

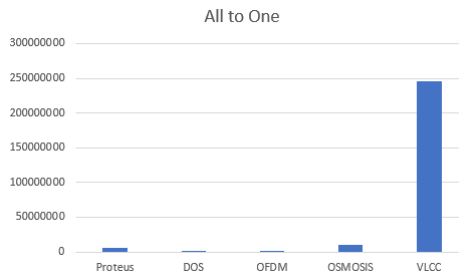


Figure 14: Throughput comparison for All to One Communication pattern

for short flows. This adds to the computational complexity of control algorithm. Optical DCNs can be reconfigurable, such architectures change the switching of a network between optical packet switching and optical circuit switching based on length of traffic flows. Changing traffic patterns can also be addressed by wavelength division multiplexing(WDM) (4). WDM dynamically configures the bandwidth of links in real time and efficiently utilizes frequency spectrum. The architectures using the reconfigurable switching WDM need control algorithm to assign wavelengths to different flows. The use of reconfigurable switching and WDM in optical DCNs increases the computational complexity of the control algorithm.

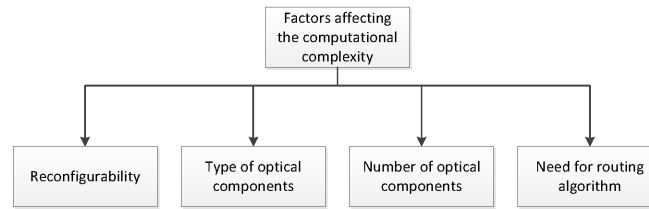


Figure 15: Factors affecting computational complexity in optical interconnects in DCNs

ii) Number of active components Optical interconnects in DCNs can have two type of optical components, active components, and passive components. The use of passive components in the architecture eliminates the need of controlling the optical components and decision-making process is simplified. However, if an optical DCN has many active optical components then each of the active components needs to be separately controlled. The timing of controlling active components is also very important. The application of control signal at a correct time increases the complexity of the control algorithm.

iii) High radix requirement Optical interconnects in DCNs need to have a high radix to support greater number of nodes connected to the network. Increasing the nodes in optical DCN increases the amount of control information to direct the packets from one node to the other. Increasing nodes affects the complexity of control algorithm. If the complexity of control algorithm increases by increasing the scale, then that architecture is not scalable to a large number of nodes.

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